REMARKS

Applicant thanks the Examiner for the very thorough consideration given the present application.

Claims 1-6 are now present in this application. Claims 1, 2, 3 and 6 are independent.

Amendments have been made to claims 1, 2, 3 and 6. Reconsideration of this application, as amended, is respectfully requested.

Examiner's Interview

Applicant conducted an interview with the Examiner on August 16, 2002 with regard to the Examiner's continued objections to the claims and disclosure (paragraphs 1, 2 and 3 of the Office Action), and the rejection under 35 U.S.C. 102(b) in paragraph 5 of the Office Action.

The Examiner stated that the rejection of claims 1-6 under 35 U.S.C. 102(b) in paragraph 5 is a typographical error. The Examiner further stated that in the "Response to Arguments" paragraph 6, the corrections to the claims and disclosure are acknowledged, and therefore, the above objections are withdrawn.

Drawings

Applicant has not received a Notice of Draftsperson's Patent Drawing

Review PTO-948 indicating whether or not the formal drawings have been approved by the Draftsperson. Clarification in the next Office Action is respectfully requested.

Rejections under 35 U.S.C. § 103

Claims 1-6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable U.S. Patent No. 5,821,587 to Jeong, for the reasons set forth in paragraph 5 of the Office Action. This rejection is respectfully traversed.

Jeong discloses an ESD circuit, denoted by the reference numeral 200 and shown in Figure1. The ESD circuit is coupled to voltage sources Vcc and Vss via field transistors Q1 and Q2, respectively. The field transistors Q1 and Q2 are coupled to a control/address pad 100. The control/address pad 100 is connected to the gate of an input transistor Q3 via a resistor Rs. An active NMOS transistor Q4 is coupled to the output of the resistor Rs and the voltage source Vss (see Jeong, Col.1, lines 36-43). When high voltage is applied to the pad 100, the field transistors Q1 and Q2 turn on, thereby causing the applied high voltage to be bypassed to the voltage source Vcc or Vss. Accordingly, the applied high voltage has no direct influence on the input transistor Q3 (see Jeong, Col.1, lines 43-49).

The Examiner states that it would have been obvious to one of ordinary skill in the art to have a resistor connected only to the input terminal (no

resistor between emitter and ground). Jeong contradicts the Examiner's assertion. As disclosed in Col.1, lines 43-49, the ESD protection circuit of Jeong operates on an entirely different theory. In the ESD protection circuit of Jeong, input transistor Q3 is protected by causing the applied high voltage to be bypassed to the voltage source Vcc or Vss. Therefore, in the ESD protection circuit of Jeong, the presence or absence of a resistor between the emitter and ground would have no effect on the operation of the circuit (since unwanted voltage is not discharged to ground). Hence, there is no motivation to modify the ESD protection circuit of Jeong to produce the Applicant's claimed ESD protection circuit.

Particularly, Jeong fails to disclose or suggest a plurality of transistors, each connected between the pad and the main chip, said transistors having a plurality of resistors connected to an input terminal, said resistors being connected in parallel with each other, and having no resistor connected between said transistors and ground, to discharge static electricity through said transistors to ground and avoid reduction in gain, as recited in independent claims 1 and 6 (as amended) or a pad formed on the second insulating film inclusive of the second contact hole and electrically connected to the buffered layer, for discharging static electricity from said pad, through the buffered layer, and through said transistor to ground, as recited in independent claims 2 and 3 (as amended). Reconsideration and withdrawal of

this art grounds of rejection are respectfully requested.

With regard to dependent claims 4 and 5, Applicant submits that claims 4 and 5 depend from independent claim 3, which is allowable for the reasons set forth above, and therefore claims 4 and 5 are allowable based on their dependence from claim 3. Reconsideration and allowance thereof are respectfully requested.

Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance.

If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone Percy L. Square, Registration No. 51,084 at (703) 205-8034, in the Washington, D.C. area.

Prompt and favorable consideration of this Amendment is respectfully requested.

Attached hereto is a marked-up version of the changes made to the application by this Amendment.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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Attachment: Version with Markings to Show Changes Made

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

The claims have been amended as follows:

1. (Twice Amended) An ESD (Electro-Static-Discharge) protection circuit comprising:

a pad and a main chip; and,

a plurality of transistors, each connected between the pad and the main chip, said transistors having a plurality of resistors connected to an input terminal, said resistors being connected in parallel with each other, and having no resistor connected between said transistors and ground, to discharge static electricity through said transistors to ground and avoid reduction in gain.

2. (Amended) An ESD protection circuit comprising:

a substrate;

a transistor formed on the substrate;

a first insulating film formed on the substrate inclusive of the transistor and having a first contact hole to an input terminal of transistor;

a buffered layer formed on the first insulating film inclusive of the first contact hole and electrically connected to the input terminal for acting as a resistor;

a second insulating film formed on the first insulating film inclusive of the buffered layer and having a second contact hole to the buffered layer; and,

a pad formed on the second insulating film inclusive of the second contact hole and electrically connected to the buffered layer, for discharging static electricity from said pad, through the buffered layer, and through said transistor to ground.

3. (Twice Amended) A method for fabricating an ESD protection circuit, comprising the steps of:

(1) forming a transistor on a substrate;

(2) forming a first insulating film on the substrate inclusive of the transistor and having a first contact hole to an input terminal of the transistor;

(3) forming a buffered layer in the first contact hole and the first insulating film in the vicinity of the first contact hole;

(4) forming a second insulating film on the first insulating film inclusive of the buffered layer and having a second contact hole to the buffered layer; and,

(5) forming a pad both on the second contact hole and the second insulating film in the vicinity of the second contact hole, for discharging static electricity from said pad, through the buffered layer, and through said transistor to ground.

6. (Amended) An ESC (Electro-Static-Discharge) protection circuit comprising:

a pad and a main chip[, said chip comprising more than one discrete component]; and

a plurality of transistors, each connected between the pad and the main chip, having resistors connected to an input terminal only, to discharge static electricity through said transistors to ground and avoid reduction in gain.